CLAIMS

WHAT IS CLAIMED IS:

1. A computer system, comprising:

a primary chassis;

a primary device having a bus for carrying electrical signals, wherein the primary device is disposed in the primary chassis;

a secondary chassis; and

an external device having a bus for carrying electrical signals, wherein the external device is disposed in the secondary chassis and the external device bus is directly electrically interconnected with the primary device bus so that the electrical signals carried on the primary device bus are transmitted to the external device bus and the electrical signals carried on the external device bus are transmitted to the primary device bus.

2. A computer system, according to claim 1, wherein the primary device is a motherboard.

3. A computer system according to claim 1, wherein the external device is a device selected from the group consisting of a storage medium, a graphics processor, and a sound processor.

4. A computer system, according to claim 1, further comprising a bridgeboard capable of directly electrically interconnecting the primary device bus and the external device bus.

5. A computer system, according to claim 4, wherein the bridgeboard further comprises a bridge chip capable of receiving signals from the primary device bus and repeating the signals over the external device bus and is capable of receiving signals from the external device bus and repeating the signals over the primary device bus.

6. A computer system, according to claim 5, wherein the bridge chip is capable of receiving the signals from the primary device bus at a first transmission speed and is capable of repeating the signals over the external device bus at a second transmission speed, and wherein the bridge chip is capable of receiving the signals from the external device bus at a second transmission speed and is capable of repeating the signals over the primary device bus at the first transmission speed

7. A computer system, according to claim 5, wherein the bridge chip is capable of translating electrical signals from a first signal protocol to a second signal protocol.

8. A computer system, according to claim 1, wherein the primary device bus is a high-speed processor bus.

9. A computer system, according to claim 1, wherein the external device bus is a high-speed processor bus.

10. A computer system, according to claim 1, further comprising a first power supply disposed in the primary chassis and a second power supply disposed in the secondary chassis, wherein the first power supply is capable of supplying power to the primary device and the second power supply is capable of supplying power to the external device.

11. A computer system, according to claim 1, further comprising a first cooling device disposed in the primary chassis and a second cooling device disposed in the secondary chassis, wherein the first cooling device is capable of cooling the primary device and the second cooling device is capable of cooling the external device

12. A method capable of sharing electrical signals, comprising:

transmitting a first electrical signal over a bus of a primary device disposed in a primary chassis;

receiving the first electrical signal over a bus of an external device disposed in a secondary chassis;

transmitting a second electrical signal over the bus of the external device disposed in the secondary chassis; and

receiving the second electrical signal over the bus of the primary device disposed in the primary chassis.

13. A method, according to claim 12, further comprising:

receiving the first electrical signal over a bus of a bridgeboard;

retransmitting the first electrical signal over the bus of the bridgeboard to the bus of the external device;

receiving the second electrical signal over the bus of the bridgeboard; and

retransmitting the second electrical signal over the bus of the bridgeboard to the bus of the primary device.

14. A method, according to claim 12, further comprising:

receiving the first electrical signal at a first transmission speed over the bus of the bridgeboard;

retransmitting the first electrical signal at a second transmission speed over the bus of the bridgeboard to the bus of the external device;

receiving the second electrical signal at the second transmission speed over the bus of the bridgeboard; and

retransmitting the second electrical signal at the first transmission speed over the bus of the bridgeboard to the bus of the primary device.

15. A method, according to claim 12, further comprising:

receiving the first electrical signal under a first signal protocol over the bus of the bridgeboard;

retransmitting the first electrical signal under a second signal protocol over the bus of the bridgeboard to the bus of the external device;

receiving the second electrical signal under the second signal protocol over the bus of the bridgeboard; and

retransmitting the second electrical signal under the first signal protocol over the bus of the bridgeboard to the bus of the primary device.

16. A computer system, comprising:

means for transmitting a first electrical signal over a bus of a primary device disposed in a primary chassis;

means for receiving the first electrical signal over a bus of an external device disposed in a secondary chassis;

means for transmitting a second electrical signal over the bus of the external device disposed in the secondary chassis; and

means for receiving the second electrical signal over the bus of the primary device disposed in the primary chassis.

17. A computer system, according to claim 16, further comprising:

means for receiving the first electrical signal over a bus of a bridgeboard;

means for retransmitting the first electrical signal over the bus of the bridgeboard to the bus of the external device;

means for receiving the second electrical signal over the bus of the bridgeboard; and

means for retransmitting the second electrical signal over the bus of the bridgeboard to the bus of the primary device.

18. A computer system, according to claim 16, further comprising:

means for receiving the first electrical signal at a first transmission speed over a bus of a bridgeboard;

means for retransmitting the first electrical signal at a second transmission speed over the bus of the bridgeboard to the bus of the external device;

means for receiving the second electrical signal at the second transmission speed over the bus of the bridgeboard; and

means for retransmitting the second electrical signal at the first transmission speed over the bus of the bridgeboard to the bus of the primary device.

19. A computer system, according to claim 16, further comprising:

means for receiving the first electrical signal under a first signal protocol over a bus of a bridgeboard;

means for retransmitting the first electrical signal under a second signal protocol over the bus of the bridgeboard to the bus of the external device;

means for receiving the second electrical signal under the second signal protocol over the bus of the bridgeboard; and

means for retransmitting the second electrical signal under the first signal protocol over the bus of the bridgeboard to the bus of the primary device.

20. A computer system, according to claim 16, further comprising means for providing power to the primary chassis and means for providing power to the secondary chassis.

21. A computer system, according to claim 16, further comprising means for providing cooling to the primary chassis and means for providing cooling to the secondary chassis.